WHAT IS CLAIMED IS:

1. A memory device, comprising:
a substrate;
a source region of said substrate;
a drain region of said substrate;
a channel region between said source and drain regions;
a thin film of nanoelements on said channel region; and
a gate contact formed on said thin film of nanoelements.

2. The memory device of claim 1, wherein said thin film of nanoelements includes a plurality of nanoparticles.

3. The memory device of claim 1, wherein said thin film of nanoelements includes a plurality of nanorods.

4. The memory device of claim 1, wherein said thin film of nanoelements includes a plurality of nanowires.

5. The memory device of claim 1, wherein said thin film of nanoelements includes at least one of nanoparticles, nanorods, and nanowires.

6. The memory device of claim 1, further comprising:
a dielectric layer between said substrate and said thin film of nanoelements.

7. The memory device of claim 1, further comprising:
a dielectric layer between said thin film of nanoelements and said gate contact.

8. The memory device of claim 1, wherein each nanoelement comprises:

a core, and

a shell that surrounds said core.

9. The memory device of claim 8, wherein said shell is an oxidized layer of said each nanoelement.

10. The memory device of claim 1, wherein said thin film of nanoelements includes nanoelements having a plurality of charge injection threshold voltages, wherein said memory device is a multistate memory device.

11. The memory device of claim 10, wherein each nanoelement comprises:

a core, and

a shell that surrounds said core.

12. The memory device of claim 11, wherein said shell is an oxidized layer of said each nanoelement.

13. The memory device of claim 11, wherein a first plurality of nanoelements of said thin film of nanoelements have shells formed to have a first thickness to cause said first plurality of nanoelements to have a first charge injection threshold voltage; and

a second plurality of nanoelements of said thin film of nanoelements have shells formed to have a second thickness to cause said second plurality of nanoelements to have a second charge injection threshold voltage.

14. The memory device of claim 11, wherein said nanoelements have a plurality of shell thicknesses to cause said nanoelements to have said plurality of charge injection threshold voltages.

15. The memory device of claim 10, wherein said nanoelements have a plurality of sizes to cause said nanoelements to have said plurality of charge injection threshold voltages.

16. The memory device of claim 15, wherein said plurality of sizes corresponds to a plurality of capacitance values for said nanoelements.

17. The memory device of claim 10, wherein discrete numbers of electrons are injected into said nanoelements according to the Coulomb blockade effect to have said plurality of charge injection threshold voltages.

18. The memory device of claim 10, wherein said nanoelements are quantum dots.

19. The memory device of claim 18, wherein a quantum confinement effect is used to create discrete energy states in said quantum dots.

20. The memory device of claim 1, wherein said source region, drain region, and channel region are configured in a p-type metal oxide semiconductor (PMOS) transistor configuration.

21. The memory device of claim 1, wherein said source region, drain region, and channel region are configured in a n-type metal oxide semiconductor (NMOS) transistor configuration.

22. The memory device of claim 1, wherein said thin film of nanoelements includes at least a monolayer of nanoelements.

23. The memory device of claim 1, wherein said thin film of nanoelements includes a plurality of layers of nanoelements.

24. The memory device of claim 1, wherein said thin film of nanoelements is a sub-monolayer of nanoelements.

25. The memory device of claim 1, wherein nanoelements of the thin film of nanoelements are covered with surface functional groups.

26. The memory device of claim 25, wherein said surface functional groups increase a separation distance between said nanoelements.

27. The memory device of claim 25, wherein said surface functional groups increase a solubility of said nanoelements.

28. A method for fabricating a memory device, comprising:

(a) forming a source region and a drain region in a substrate thereby defining a channel region therebetween;

(b) forming a thin film of nanoelements on the channel region; and

(c) forming a gate contact on the thin film of nanoelements.

29. The method of claim 28, wherein the thin film of nanoelements includes a plurality of nanoparticles, wherein step (b) comprises:

depositing the plurality of nanoparticles on the substrate.

30. The method of claim 28, wherein the thin film of nanoelements includes a plurality of nanorods, wherein step (b) comprises:

depositing the plurality of nanorods on the substrate.

31. The method of claim 28, wherein the thin film of nanoelements includes a plurality of nanowires, wherein step (b) comprises:

depositing the plurality of nanorods on the substrate.

32. The method of claim 28, wherein the thin film of nanoelements includes a mixture of nanoparticles, nanorods, and nanowires, wherein step (b) comprises:

depositing the plurality of mixture of nanoparticles, nanorods, and nanowires on the substrate.

33. The method of claim 28, further comprising:

(d) prior to step (b), forming a dielectric layer on the substrate.

34. The method of claim 28, further comprising:

(d) prior to step (c), forming a dielectric layer on the thin film of nanoelements.

35. The method of claim 28, further comprising:

(d) forming each nanoelement to have a core and a shell, wherein the shell surrounds the core for each nanoelement.

36. The method of claim 35, wherein step (d) comprises:

oxidizing each nanoelement to form the shell as an oxidized layer around the core for each nanoelement.

37. The method of claim 28, wherein the thin film of nanoelements includes nanoelements having a plurality of charge injection threshold voltages, wherein step (b) comprises:

(b) forming on the channel region the thin film of nanoelements that includes nanoelements having the plurality of charge injection threshold voltages.

38. The method of claim 37, further comprising:

(d) forming each nanoelement to have a core and a shell, wherein the shell surrounds the core for each nanoelement.

39. The method of claim 38, wherein step (d) comprises:

oxidizing each nanoelement to form the shell as an oxidized layer around the core for each nanoelement.

40. The method of claim 38, wherein step (d) comprises:

forming a first plurality of nanoelements of the thin film of nanoelements to have shells of a first thickness to cause the first plurality of nanoelements to have a first charge injection threshold voltage; and

forming a second plurality of nanoelements of the thin film of nanoelements to have shells of a second thickness to cause the second plurality of nanoelements to have a second charge injection threshold voltage.

41 The method of claim 38, wherein step (d) comprises:

forming the nanoelements have a plurality of shell thicknesses to cause the nanoelements to have the plurality of charge injection threshold voltages.

42. The memory device of claim 37, further comprising:

(d) forming the nanoelements to have a plurality of sizes to cause said nanoelements to have the plurality of charge injection threshold voltages.

43. The memory device of claim 42, wherein step (d) comprises:

selecting the plurality of sizes to correspond to a plurality of capacitance values for the nanoelements.

44. The memory device of claim 37, further comprising:

using the Coulomb blockade effect to cause the nanoelements to have the plurality of charge injection threshold voltages.

45. The memory device of claim 37, wherein the thin film of nanoelements includes a plurality of quantum dots, wherein step (b) comprises:

depositing the plurality of quantum dots on the substrate.

46. The memory device of claim 45, further comprising:

using a quantum confinement effect to create discrete energy states in said quantum dots.

47. The method of claim 23, further comprising:

(d) doping the substrate.

48. The method of claim 23, wherein step (a) comprises:

doping the source region and drain region with an n-type dopant to configure the memory device in an n-type metal oxide semiconductor (NMOS) transistor configuration.

49. The method of claim 23, wherein step (a) comprises:

doping the source region and drain region with a p-type dopant to configure the memory device in an p-type metal oxide semiconductor (PMOS) transistor configuration.

50. The method of claim 23, further comprising:

treating the nanoelements with a surface treatment.

51. The method of claim 50, further comprising:

allowing said surface treatment to increase a separation distance between the nanoelements.

52. The method of claim 50, wherein said surface treatment improves a solubility of the nanoelements.

53. An apparatus for printing, comprising:

an electrode; and

a charge diffusion layer having

a first surface and a second surface, wherein said second surface is coupled to said electrode, wherein an electrical potential difference is maintained between said electrode and said first surface of said charge diffusion layer, and

a matrix containing a plurality of nanoelements configured to be anisotropically electrically conductive between said first surface and said second surface to transfer charge through said charge diffusion layer to areas of said first surface.

54. The apparatus of claim 53, further comprising:

a photoconductor layer coupled between said second surface of said charge diffusion layer and said electrode, wherein the photoconductor layer supplies charge to said second surface of said charge diffusion layer for transfer through said charge diffusion layer.

55. The apparatus of claim 54, further comprising optics that produce light defining a latent image, wherein said light is received at said photoconductor layer, wherein an amount of said charge supplied by said photoconductor layer is proportional to said light received at said photoconductor layer.

56. The apparatus of claim 55, wherein said light is received at said photoconductive layer through said electrode.

57. The apparatus of claim 55, wherein said light is received at said photoconductive layer through said charge diffusion layer.

58. The apparatus of claim 53, wherein said nanoelements are photoconductive.

59. The apparatus of claim 58, further comprising optics that produce light defining a latent image, wherein said light is received at said charge diffusion layer, wherein said nanoelements produce an amount of said charge proportional to said received light.

60. The apparatus of claim 59, wherein said light is received at said charge diffusion layer through said electrode.

61. The apparatus of claim 69, wherein said light is received at said charge diffusion layer through said first surface of said charge diffusion layer.

62. The apparatus of claim 53, further comprising a coating layer disposed on said first surface, wherein said charge is transferred from said areas of said first surface to corresponding areas of said coating layer.

63. The apparatus of claim 62, wherein when toner is applied to said coating layer, toner adheres to charged areas of said coating layer, wherein a target print surface can be applied to said coating layer to receive said toner in areas of said target print surface corresponding to said areas of said coating layer to which toner adheres.

64. The apparatus of claim 53, wherein when toner is applied to said first surface, toner adheres to areas of said first surface that are charged, wherein a target print surface can be applied to said first surface to receive said toner in areas of said target print surface corresponding to said areas of said first surface to which toner adheres.

65. The apparatus of claim 64, wherein said first surface of said charge diffusion layer is polished to create a smooth first surface.

66. The apparatus of claim 53, wherein the apparatus is a laser printer.

67. The apparatus of claim 54, wherein the apparatus is a photocopier.

68. The apparatus of claim 54, further comprising a light source.

69. The apparatus of claim 68, wherein the light source includes a liquid crystal diode array.

70. The apparatus of claim 58, wherein the light source includes at least one light emitting diode.

71. The apparatus of claim 68, wherein the light source includes a laser.

72. The apparatus of claim 53, further comprising a digital micromirror device (DMD).

73. The apparatus of claim 53, wherein the apparatus prints in color.

74. The apparatus of claim 53, wherein the apparatus prints in black and white.

75. The apparatus of claim 53, wherein said thin film of nanoelements includes a plurality of nanoparticles.

76. The apparatus of claim 53, wherein said thin film of nanoelements includes a plurality of nanorods.

77. The apparatus of claim 53, wherein said thin film of nanoelements includes a plurality of nanowires.

78. The apparatus of claim 53, wherein said nanoelements are made from a semiconducting material.

79. The apparatus of claim 53, wherein said nanoelements are made from a metal.

80. The apparatus of claim 53, wherein each nanoelement includes a core portion and a shell portion that surrounds said core portion, wherein a first end and a second end of said core portion is exposed through said shell portion.

81. The apparatus of claim 80, wherein said shell portion is electrically insulating.

82. The apparatus of claim 56, wherein said electrode is made from a transparent conductor.

83. The apparatus of claim 60, wherein said electrode is made from a transparent conductor.

84. A method for manufacturing a printing device, comprising:

forming a charge diffusion layer that includes a matrix containing a plurality of electrically conductive nanoelements that are anisotropically conductive between a first surface and a second surface of the charge diffusion layer;

coupling an electrode to the second surface of the charge diffusion layer; and

coupling a voltage source to the electrode to create an electrical potential difference between the electrode and first surface of the charge diffusion layer during operation of the printing device.

85. The method of claim 84, further comprising:

coupling a photoconductor layer between the second surface of the charge diffusion layer and the electrode.

86. The method of claim 85, further comprising:

configuring optics to produce light defining a latent image, such that the produced light is received at the photoconductor layer.

87. The method of claim 84, wherein the nanoelements are photoconductive, further comprising:

configuring optics to produce light defining a latent image, such that the produced light is received at the charge diffusion layer.

88. The method of claim 84, further comprising:

forming a coating layer on the first surface.

89. The method of claim 84, further comprising:

polishing the first surface of said charge diffusion layer.